

## REMARKS

This application has been reviewed in light of the Office Action dated June 9, 2008.

Claims 1 and 3-7 are presented for examination. Claims 2 and 8-18 were previously cancelled without prejudice. Claim 1, which is the only independent claim, has been amended. Favorable review is respectfully requested.

Claim 1 recites an integrated circuit device having an electrically active surface and an opposing backside surface and sides extending therebetween. The sides include at least one feature that is effective to limit the ingress of moisture along an interface between said integrated circuit device and a dielectric molding resin. Claim 1 has been amended to recite that this interface has an end portion between the integrated circuit device at the exposed backside surface and the dielectric molding resin adjacent thereto, and an interior portion substantially parallel to the backside surface. Support for this claim language appears in the specification at least at paragraph 0023 of the published application, with reference to FIG. 2. In the embodiment shown in FIG. 2, the interface 28 between device 12 and molding resin 26 has an end portion between the exposed backside 14 and the molding resin (see arrowhead of lead line from numeral 28), and an interior portion parallel to backside surface 14. This interior portion intersects sidewall 58. As noted previously (in the Amendment dated February 13, 2008), the interface 28 is not a straight line, but rather an extended path.

Claims 1 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Seo et al. (U.S. Pat. No. 6,858,919) in view of Minamio et al. (U.S. Pat. No. 6,680,524). The applicants respectfully submit that independent claim 1 is patentable over the cited art, for the following reasons.

As noted above, claim 1 recites an integrated circuit device where sides thereof include a feature effective to limit the ingress of moisture along an interface between the device and a dielectric molding resin. The backside surface of the device is exposed; an end portion of the interface is between the device at the exposed backside surface and the molding resin, and an interior portion of the interface is substantially parallel to the backside surface. This is contrary to the teaching of Seo et al., in which the chip device has only straight sides. The straight sides of Seo et al. define interfaces leading in straight lines directly away from the backside of the

chip, as opposed to along extended paths. Accordingly, Seo et al. does not and cannot suggest an interface having an interior portion, as recited in claim 1.

The Examiner points to Minamio et al. as disclosing a semiconductor package with the features of claim 1. The applicants wish to point out that in the arrangement of Minamio et al., the device is completely encapsulated by resin and a wiring substrate (see FIGS. 4 and 14). This is contrary to claim 1, which explicitly recites an exposed backside surface of an integrated circuit device. Modifying the device of Seo et al. in accordance with Minamio et al. would involve covering the backside surface of the semiconductor device with encapsulating resin. This would defeat the object of improving thermal dissipation in the device package, and thus render the combination unsuitable for its intended purpose. The combination thus cannot render the claim obvious. MPEP § 2143.01(V).

Furthermore, since the sides and backside of the Minamio et al. device are completely encapsulated, it follows that an interface between the device and the resin cannot have an end portion at the exposed backside (compare Minamio et al. FIG. 4 with FIG. 2 of the specification). Accordingly, Minamio et al. does not disclose or suggest an interface as recited in claim 1, and thus does not remedy the above-noted defect of Seo et al. as a reference against the claim. Claim 1 is not rendered obvious by either of the cited references, or by a combination thereof.

Claims 3 and 5-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Seo et al. and Minamio et al. in view of Masumoto et al.(U.S. Pat. No. 6,759,745), Kinsman (U.S. Pat. No. 6,700,206), and/or Okada et al.(U.S. Pat. No. 7,192,798). The applicants have not found in any of the three additional references any teaching or suggestion of an interface as recited in amended claim 1. Specifically, there is no interface between a device and an encapsulating material having an end portion at an exposed surface in Masumoto et al. or Kinsman.

Masumoto et al. discloses (col. 4, line 63) that the surface of the integrated circuit device that adheres to other features of the package is smaller than the opposing other side of the integrated circuit device. This is contrary to applicants' embodiments, as illustrated in FIG. 2 of the specification where the surface 16 attached to other package features has a larger surface area than the opposing side. As disclosed in the Abstract of Masumoto et al., the smaller surface is intended to limit fillet spread out around the semiconductor chip. It is further noted that in no embodiments of Masumoto et al. does any surface of the integrated circuit device form a portion

of the package surface. Masumoto et al. does not include an interface extending to a surface of the package, and thus cannot suggest an interface having an end portion as recited in claim 1.

Masumoto et al. teach away from applicants' claims in that the surface of the integrated circuit device bonded to other features has a smaller surface area of than the opposing other side, while in applicants' claims the surface bonded to other features has a larger surface area than the backside that forms a portion for the package. Further, as Masumoto et al. do not have an interface extending to the package surface, there is nothing in the combination of Seo et al. and Masumoto et al. to teach or suggest features to limit the ingress of moisture along the interface and to mechanically lock the integrated circuit device to the dielectric molding resin.

Similarly, Kinsman is understood to disclose a packaged device in which the device is fully encapsulated (see Kinsman, FIGS. 2 and 6C). As discussed above, this is contrary to claim 1, which requires a backside surface and electrical contacts exposed on opposing sides of the package.

Okada et al. is understood to disclose an exposed surface in which a sensor is formed. This is not understood to be an "opposing backside surface," opposite to an electrically active surface, as recited in claim 1. Furthermore, Okada et al. does not disclose or suggest that the sides of the device have a feature as recited in claim 1 and discussed above. In particular, the sides of the Okada et al. integrated circuit are straight and do not include any features effective to limit the ingress of moisture along an interface between the integrated circuit device and the molding resin, nor to mechanically lock the integrated circuit device to the molding resin. Accordingly, claim 1 is not rendered obvious by any of these additional references (considered either alone or in combination with Seo et al. and Minamio et al.).

In view of the foregoing amendments and remarks, favorable reconsideration and early passage to issue of the present application are respectfully requested.

If the Examiner has any questions or believes that a discussion with Applicants' attorney would expedite prosecution, the Examiner is invited and encouraged to contact the undersigned at the telephone number below.

This Amendment is being submitted on the first business day following the expiration of two months from the date of the final Office Action. Accordingly, the period for reply will expire at three months from the date of the Office Action or on the date an Advisory Action is mailed, whichever is later. MPEP § 706.07(f).

No fee is believed to be due. The Commissioner nevertheless is authorized to charge any required fees to Deposit Account No. 23-1665. All correspondence should continue to be directed to the address given below, which is the address associated with Customer Number 27267.

Respectfully submitted,

  
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Date: August 11, 2008

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